IN THE CLAIMS

Please cancel claim 30, and further amend the claims as shown below.

1-15. (Canceled)

16. (Currently amended) Method to implement a column interleaving function, comprising the steps of:

providing a number of memories equal to the maximum number of columns in the interleaving ~~function,~~ function;

inputting a stream of data entities~~,~~ into a shift register;

writing said data entities successively from said shift register into a memory, until all memories are completely filled or until all data entities are ~~written,~~ written;

performing selection and permutation on said ~~memories, and~~ memories; and

reading out said data entities in said permuted memories, in a memory-by-memory fashion.

17. (Currently amended) Method as in claim 16, wherein ~~data entities in the input stream are first written into a register and when said register is filled,~~ the step of writing into a memory is applied when said shift register is filled.

18. (Previously presented) Method as in claim 16, wherein said data entities are logical ones and zeros.

19. (Previously presented) Method as in claim 16, wherein said data entities are multiple bit words.

20. (Previously presented) Method as in claim 16, wherein said data entities are three bit words.

21. (Currently amended) Method as in claim 17, wherein said shift register is arranged to store each multiple bit word at one location in said memories.

22. (Previously presented) Method as in claim 16, wherein the number of columns used in the column interleaving function is changed on the fly, said number of columns not exceeding said maximum number of columns.

23. (Currently amended) A module ~~for column interleaving~~ comprising:

~~means for implementing a column interleaving function, wherein the means for implementing the column interleaving function comprises:~~

a number of memories equal to the maximum number of columns in ~~the interleaving function,~~ a column interleaving function;

~~means for inputting~~ a shift register that receives a stream of data ~~entities,~~ entities; and

a controller that controls:

~~means for~~ writing said data entities successively into a memory, until all memories are completely filled or until all data entities are ~~written,~~ written;

~~means for performing~~ selection and permutation on said ~~memories, and~~ memories; and

~~means for~~ reading out said data entities in said permuted memories, in a memory-by-memory fashion.

24. (Previously presented) A communication system device, comprising a module as in claim 23.

25. (Previously presented) A spread-spectrum communication apparatus comprising a module as in claim 23.

26. (Currently amended) An integrated circuit device comprising:

~~a module for column interleaving, said module comprising means for implementing a column interleaving function, wherein the means for implementing the column interleaving function comprises:~~

a number of memories equal to the maximum number of columns in ~~the interleaving function,~~ a column interleaving function;

~~means for inputting~~ a shift register that receives a stream of data ~~entities,~~ entities; and

a sub-circuit that controls:

~~means for~~ writing said data entities successively from said shift register into a memory, until all memories are completely filled or until all data entities are ~~written,~~ written;

~~means for performing~~ selection and permutation on said ~~memories, and~~ memories; and

~~means for~~ reading out said data entities in said permuted memories, in a memory-by-memory fashion.

27. (Previously presented) A communication system device, comprising an integrated circuit device as in claim 26.

28. (Previously presented) A spread-spectrum communication apparatus comprising an integrated circuit device as in claim 26.

29. (Currently amended) A column interleaver, comprising:

a number of memories equal to the maximum number of columns desired in the interleaver;

a shift register that receives a stream of data entities; and

a module that controls (a) writing of said data entities from said shift register to said memories ~~and means to perform~~, and (b) column selection and permutation.

30. (Canceled)

Please add the following claims, newly numbered as claims 31 - 37.

31. (New) The method of claim 16, wherein said shift register is a parallel shift register.

32. (New) The module of claim 23, wherein said controller controls said writing to occure when said shift register is filled.

33. (New) The module of claim 23, wherein said shift register is a parallel shift register.

34. (New) The integrated circuit device of claim 26, wherein said sub-circuit controls said writing to occur when said shift register is filled.

35. (New) The integrated circuit of claim 26, wherein said shift register is a parallel shift register.

36. (New) The column interleaver of claim 29, wherein said module controls said writing to occur when said shift register is filled.

37. (New) The column interleaver of claim 29, wherein said shift register is a parallel shift register.